WHAT IS CLAIMED IS:

Claim 1 (Original): A semiconductor device comprising:

a channel region of a first conductivity provided in a surface of a semiconductor substrate;

a source region of a second conductivity different from the first conductivity, the source region being provided on an edge of a trench which extends through the channel region;

a gate oxide film provided on an interior wall of the trench; and

a gate electrode provided in the trench in opposed relation to the channel region with the intervention of the gate oxide film;

wherein the interior wall of the trench includes a first interior side surface having a (100) plane orientation, and a second interior side surface having a plane orientation different from the plane orientation of the first interior side surface;

wherein the source region is disposed away from a portion of the gate oxide film provided on the second interior side surface.

Claim 2 (Original): A semiconductor device as set forth in claim 1, wherein the interior wall of the

trench further include a bottom surface having a major plane orientation with a higher areal atom density than the first interior side surface.

Claim 3 (Original): A semiconductor device as set forth in claim 2, wherein the surface of the semiconductor substrate has a plane orientation with a greater areal atom density than the surface having the (100) plane orientation.

Claim 4 (Original): A semiconductor device as set forth in claim 2, wherein the surface of the semiconductor substrate has a (110) plane orientation.

Claim 5 (Original): A semiconductor device as set forth in claim 1,

wherein the trench includes a plurality of trench portions extending parallel to each other along the first interior side surface in the surface of the semiconductor substrate,

the semiconductor device further comprising a lower resistance region of the first conductivity extending longitudinally of the trench portions and intervening between the second interior side surface and the source region, the lower resistance region being imparted with

a lower resistance by introduction of an impurity.

Claim 6 (Original): A semiconductor device as set forth in claim 1, wherein the first interior side surface has a greater length as measured along the surface of the semiconductor substrate than the second interior side surface.